Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] 1. A thin film transistor array, comprising:
a substrate;
a plurality of scan lines, disposed over the substrate;
a plurality of data lines, disposed over the substrate, wherein the substrate is defined into a plurality of pixel areas by the scan lines and the data lines;
a plurality of thin film transistor, driven by the scan lines and the data lines, wherein each thin film transistor is disposed in one of the pixel areas correspondingly;
a plurality of pixel electrodes, wherein each pixel electrode is disposed in one of the pixel areas and is electrically connected to one of the thin film transistors correspondingly, a portion of each pixel electrode is located above one of the scan lines;
a plurality of bottom electrodes, each bottom electrode is disposed between one of the pixel electrodes and one of the scan lines; and
a plurality of connecting conductive layers, each connecting conductive layer is located over and electrically connected between one of the bottom electrodes and one of the scan lines correspondingly.

[c2] 2. The thin film transistor array of claim 1, further comprising a passivation layer disposed between the pixel electrodes and the bottom electrodes as well as the connecting conductive layer and the bottom electrodes.

[c3] 3. The thin film transistor array of claim 2, further comprising a dielectric layer disposed between the bottom electrodes and the scan lines.

[c4] 4. The thin film transistor array of claim 3, wherein the passivation layer and the dielectric layer comprise a plurality of first contact windows and a plurality of second contact windows, and each first contact window exposes one of the bottom electrode, and each second contact window exposes one of the scan lines.

[c5] 5. The thin film transistor array of claim 4, wherein each connecting conductive layer is electrically connected to one of the bottom electrodes through one of the first contact windows, and each connecting conductive layer is electrically connected to one of the scan lines through one of the second contact windows.

[c6] 6. The thin film transistor array of claim 3, wherein the passivation layer and the dielectric layer comprise a plurality of third contact windows, and each third contact window exposes one of the bottom electrode and one of

the scan lines simultaneously.

[c7] 7. The thin film transistor array of claim 6, wherein each connecting conductive layer is electrically connected to one of the bottom electrodes and one of the scan lines through one of the third contact windows simultaneously.

[c8] 8. The thin film transistor array of claim 1, wherein the material of the connecting conductive layers is the same as the material of the pixel electrodes.

[c9] 9. The thin film transistor array of claim 8, wherein the material of the connecting conductive layers and the pixel electrodes comprises ITO or IZO.

[c10] 10. A thin film transistor array, comprising:
a substrate;
a plurality of scan lines, disposed over the substrate;
a plurality of data lines, disposed over the substrate, wherein the substrate is divided to a plurality of pixel areas by the scan lines and the data lines;
a plurality of thin film transistor, driven by the scan lines and the data lines, wherein each thin film transistor is disposed in one of the pixel areas correspondingly;
a plurality of pixel electrodes, wherein each pixel electrode is disposed in one of the pixel areas and is electri-

cally connected to one of the thin film transistors correspondingly;

a plurality of common lines, disposed over the substrate, wherein a portion of each pixel electrode is located above one of the common lines;

a plurality of bottom electrodes, each bottom electrode is disposed between one of the pixel electrodes and one of the common lines; and

a plurality of connecting conductive layers, each connecting conductive layer is located over and electrically connected between one of the bottom electrodes and one of the common lines correspondingly.

[c11] 11. The thin film transistor array of claim 10, further comprising a passivation layer disposed between the pixel electrodes and the bottom electrodes as well as the connecting conductive layer and the bottom electrodes.

[c12] 12. The thin film transistor array of claim 11, further comprising a dielectric layer disposed between the bottom electrodes and the common lines.

[c13] 13. The thin film transistor array of claim 12, wherein the passivation layer and the dielectric layer comprise a plurality of first contact windows and a plurality of second contact windows, and each first contact window exposes one of the bottom electrode, and each second

contact window exposes one of the common lines.

[c14] 14. The thin film transistor array of claim 13, wherein each connecting conductive layer is electrically connected to one of the bottom electrodes through one of the first contact windows, and each connecting conductive layer is electrically connected to one of the common lines through one of the second contact windows.

[c15] 15. The thin film transistor array of claim 12, wherein the passivation layer and the dielectric layer comprise a plurality of third contact windows, and each third contact window exposes one of the bottom electrode and one of the common lines simultaneously.

[c16] 16. The thin film transistor array of claim 15, wherein each connecting conductive layer is electrically connected to one of the bottom electrodes and one of the common lines through one of the third contact windows simultaneously.

[c17] 17. The thin film transistor array of claim 10, wherein the material of the connecting conductive layers is the same as the material of the pixel electrodes.

[c18] 18. The thin film transistor array of claim 17, wherein the material of the connecting conductive layers and the pixel electrodes comprises ITO or IZO.